
# PSMN071-100NSE

## N-channel 100 V, 82 mOhm standard level ‘ASFET with enhanced SOA’ in DFN2020 package. Recommended for fault tolerant applications including PoE, inrush management, eFuse and relay replacement

**2 October 2023** **Preliminary data sheet**

## 1. General description

New standards and proprietary approaches are enabling Power-over-Ethernet (PoE) systems capable of delivering up to 90 W to each powered device (PD). Such solutions place increased demands on the power sourcing equipment (PSE) in terms of “soft-start”, thermal management and power density requirements. These ASFETs combine enhanced SOA in a compact 2 mm x 2 mm footprint making them ideally placed for a variety of applications including PoE, eFuse and relay replacement.

## 2. Features and benefits

- Enhanced safe operating area (SOA) for superior linear mode operation
- Low $R_{DSon}$ for low $I^2R$ conduction losses
- 2 mm x 2 mm space-saving DFN2020 package, 60% smaller footprint than LFPAK33
- Very low $I_{DSS}$ leakage

## 3. Applications

- Low power PoE applications
- IEEE802.3at and proprietary PoE solutions
- Fault tolerant load switch - inrush management and eFuse applications
- Battery management applications
- Relay replacement
- WIFI hotspots
- 5G picocells
- CCTV

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 100 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | | - | - | 12.7 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 31 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 25 °C; Fig. 11 | | - | 67 | 82.3 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 175 °C; Fig. 12 | | - | 149 | 187 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 5 A; $V_{DS}$ = 50 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | 0.3 | 1 | 2.3 | nC |
| $Q_{G(tot)}$ | total gate charge | | | 3.1 | 6.3 | 9.5 | nC |

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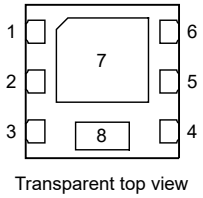
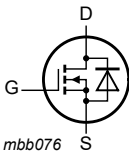
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Avalanche ruggedness** | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 8 A; $V_{sup}$ ≤ 100 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 15 µs; Fig. 4 | [1] | - | - | 7.6 | mJ |
| **Source-drain diode** | | | | | | | |
| $Q_r$ | recovered charge | $I_S$ = 5 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 50 V; $T_j$ = 25 °C; Fig. 17 | | - | 21.8 | - | nC |

[1] Protected by 100% test

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | D | drain |  Transparent top view **DFN2020M-6 (SOT1220-2)** |  |
| 2 | D | drain | | |
| 3 | G | gate | | |
| 4 | S | souce | | |
| 5 | D | drain | | |
| 6 | D | drain | | |
| 7 | D | drain | | |
| 8 | S | souce | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN071-100NSE | DFN2020M-6 | plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm | SOT1220-2 |

## 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PSMN071-100NSE | ZU |

## 8. Limiting values

**Table 5. Limiting values**

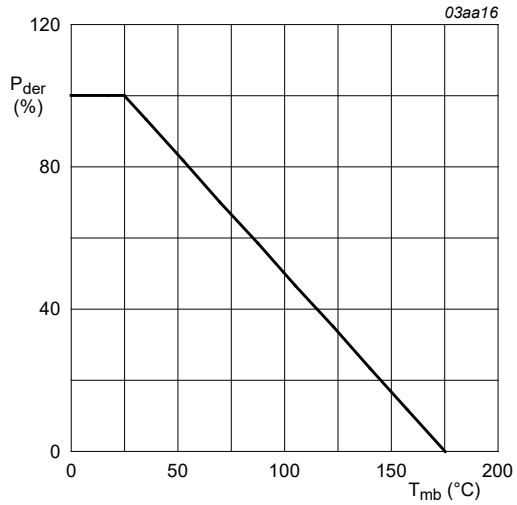
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 100 | V |
| $V_{DGR}$ | drain-gate voltage | 25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ | | - | 100 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 31 | W |

**N-channel 100 V, 82 mOhm standard level 'ASFET with enhanced SOA' in DFN2020 package. Recommended for fault tolerant applications including PoE, inrush management, eFuse and relay**

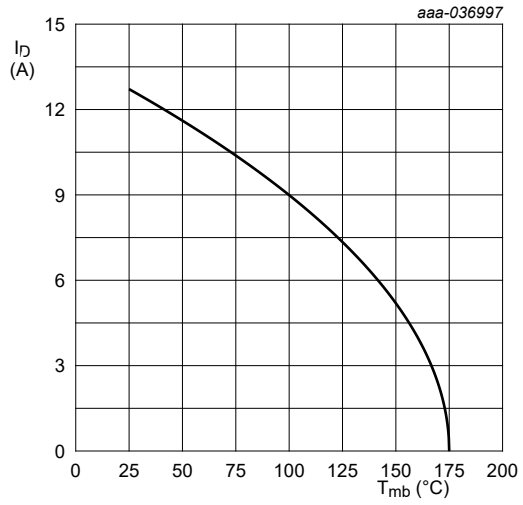
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | | - | 12.7 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | | - | 9 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p \leq$ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 51 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 12.7 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq$ 10 µs; $T_{mb}$ = 25 °C | | - | 51 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 8 A; $V_{sup} \leq$ 100 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 15 µs; Fig. 4 | [1] | - | 7.6 | mJ |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup} \leq$ 100 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $R_{GS}$ = 50 Ω; Fig. 4 | [1] | - | 8 | A |

[1] Protected by 100% test



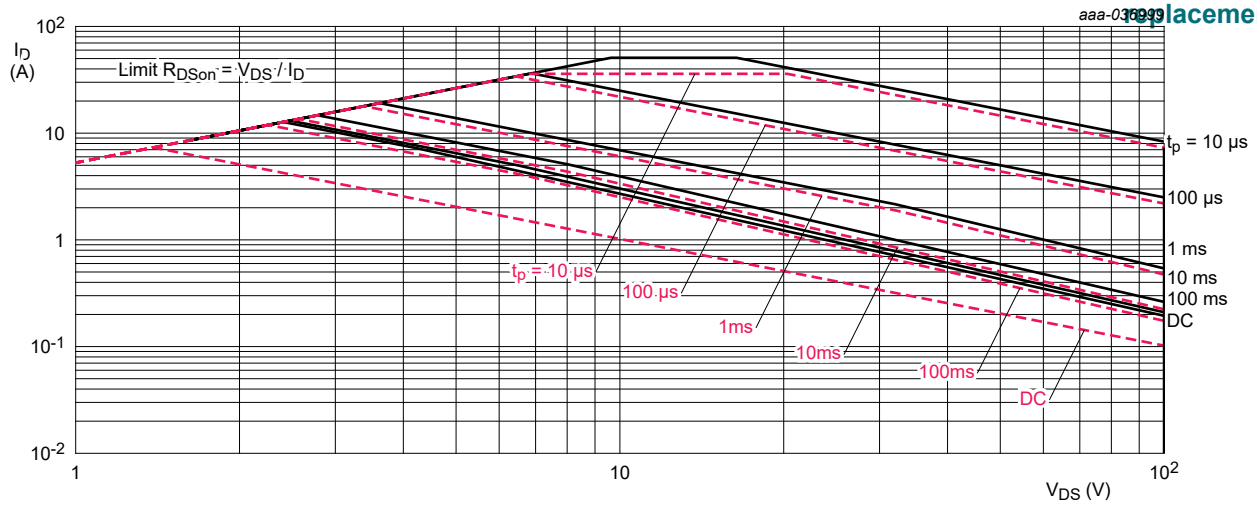

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



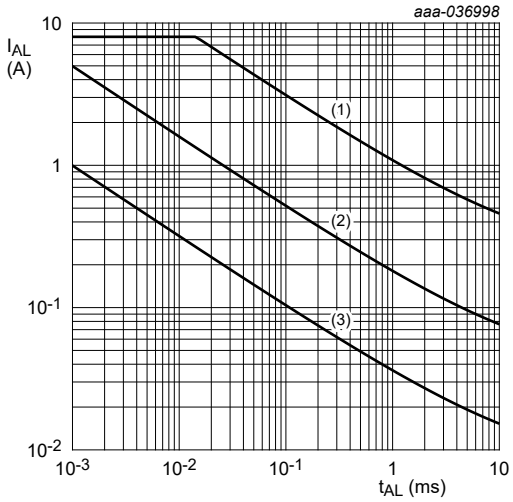

$V_{GS} \geq$ 10 V

**Fig. 2. Continuous drain current as a function of mounting base temperature**




$T_{mb}$ = 25 °C (solid black line); $T_{mb}$ = 125 °C (red dashed line); $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**




(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time**

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | 4.5 | 4.9 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | Fig. 6 | | - | 63 | - | K/W |
| | | Fig. 7 | | - | 239 | - | K/W |

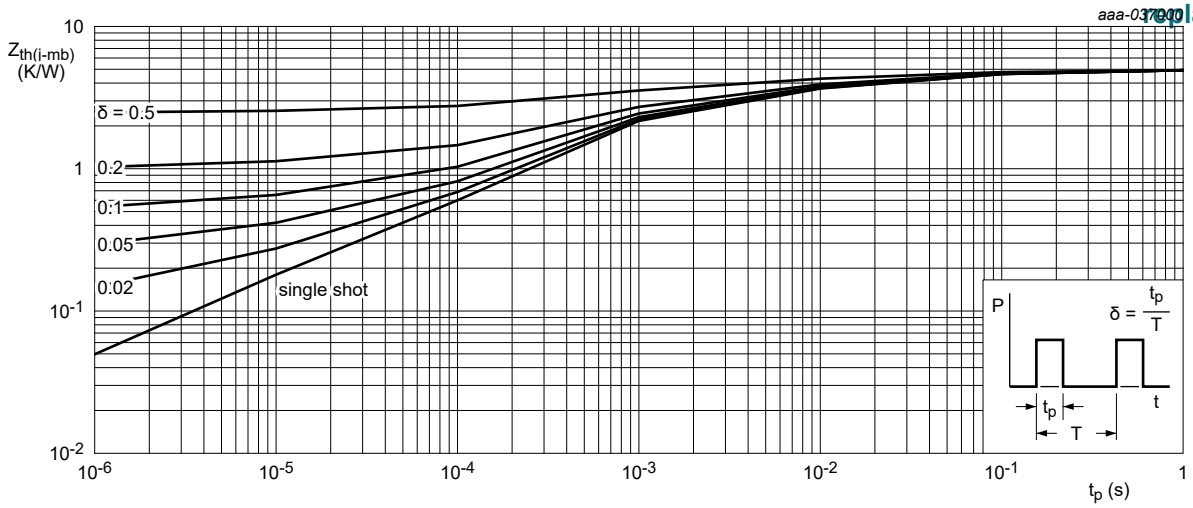
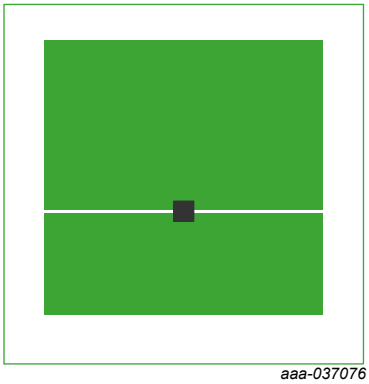
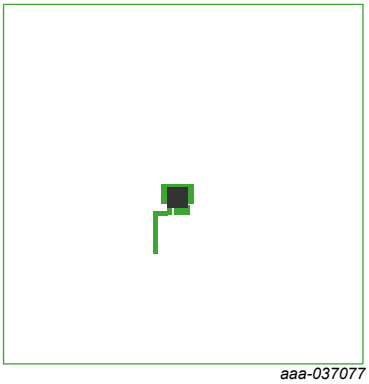



**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**




Copper square 25.4 mm square; 70 µm thick on FR4 board

**Fig. 6. PCB layout for thermal resistance from junction to ambient**




70 µm thick copper on FR4 board

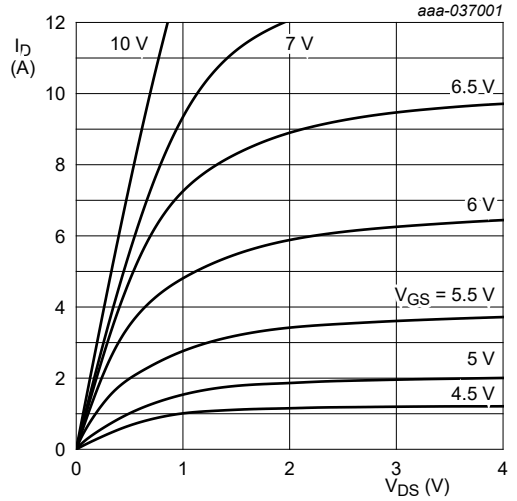
**Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient**

## 10. Characteristics

**Table 7. Characteristics**

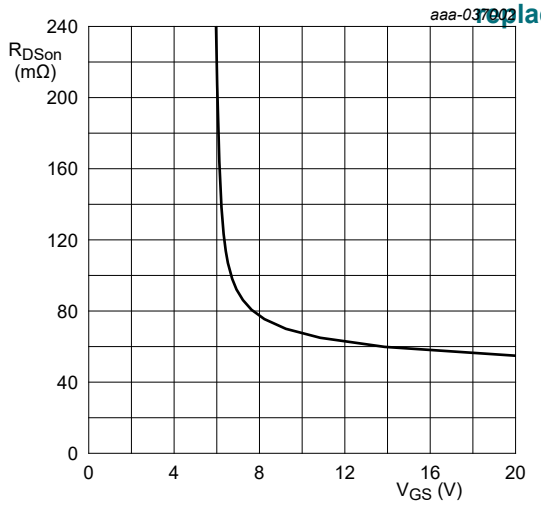
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 100 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 90 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C | | 2 | 2.6 | 3.6 | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 175 °C | | - | 1.7 | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = -55 °C | | - | 3 | - | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | 25 °C ≤ $T_j$ ≤ 150 °C | | - | -4.2 | - | mV/K |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 100 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.01 | 1 | µA |
| | | $V_{DS}$ = 100 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | 0.7 | 100 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 25 °C; Fig. 11 | | - | 67 | 82.3 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 100 °C; Fig. 12 | | - | 104 | 131 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 5 A; $T_j$ = 175 °C; Fig. 12 | | - | 149 | 187 | mΩ |
| $R_G$ | gate resistance | f = 1 MHz; $T_j$ = 25 °C | | 0.4 | 0.8 | 1.6 | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 5 A; $V_{DS}$ = 50 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | 3.1 | 6.3 | 9.5 | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C | | - | 5.7 | - | nC |
| $Q_{GS}$ | gate-source charge | $I_D$ = 5 A; $V_{DS}$ = 50 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | 1.7 | 2.8 | 3.9 | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | - | 1.42 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | - | 1.37 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | 0.3 | 1 | 2.3 | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 5 A; $V_{DS}$ = 50 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | - | 5.7 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 50 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 15 | | 239 | 399 | 559 | pF |
| $C_{oss}$ | output capacitance | | | 57 | 95 | 152 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | 0.4 | 4.2 | 11 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 50 V; $R_L$ = 10 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 5 Ω; $T_j$ = 25 °C | | - | 3.4 | - | ns |
| $t_r$ | rise time | | | - | 2.3 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 5.1 | - | ns |
| $t_f$ | fall time | | | - | 4.6 | - | ns |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 5 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 16 | | - | 0.92 | 1 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 5 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 50 V; $T_j$ = 25 °C; Fig. 17 | | - | 29.4 | - | ns |
| $Q_r$ | recovered charge | | | - | 21.8 | - | nC |



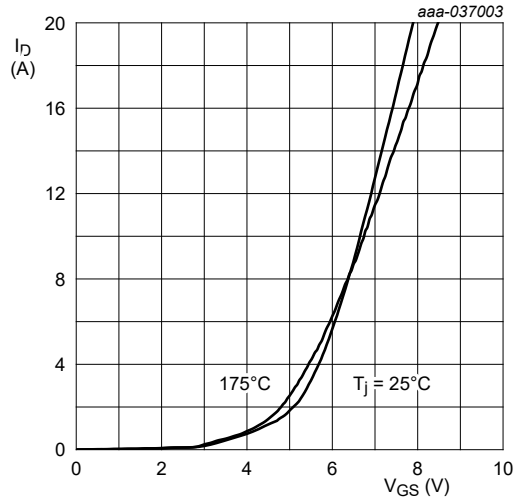

$T_j$ = 25 °C

**Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values**



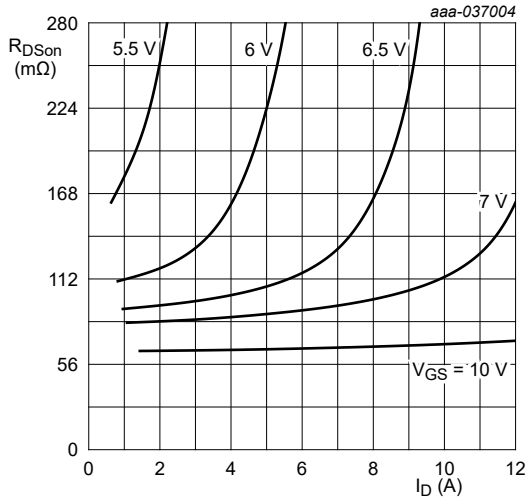

$T_j$ = 25 °C; $I_D$ = 5 A

**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



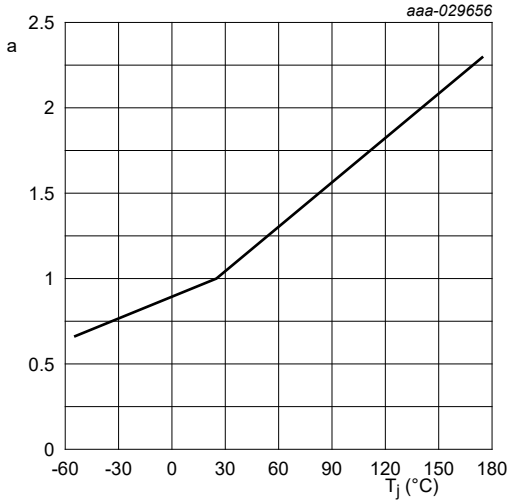

$V_{DS}$ = 8 V

**Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



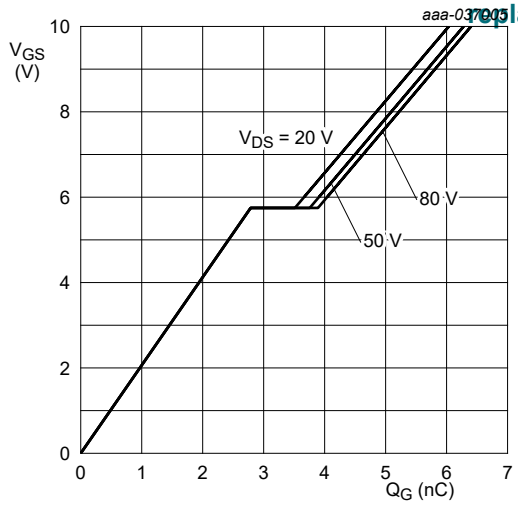

$T_j$ = 25 °C

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**




$T_j$ = 25 °C; $I_D$ = 5 A

**Fig. 13. Gate-source voltage as a function of gate charge; typical values**

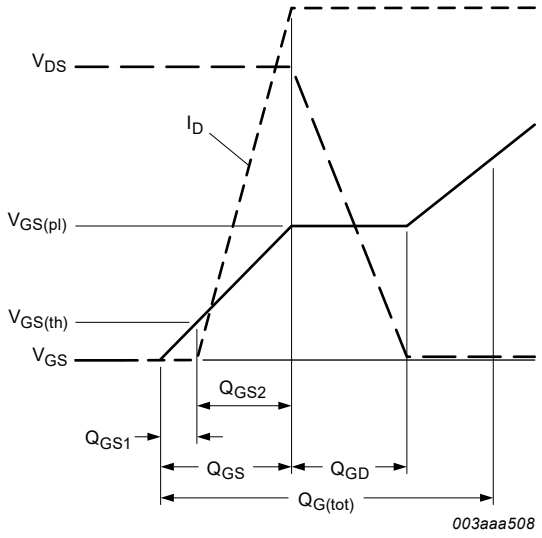
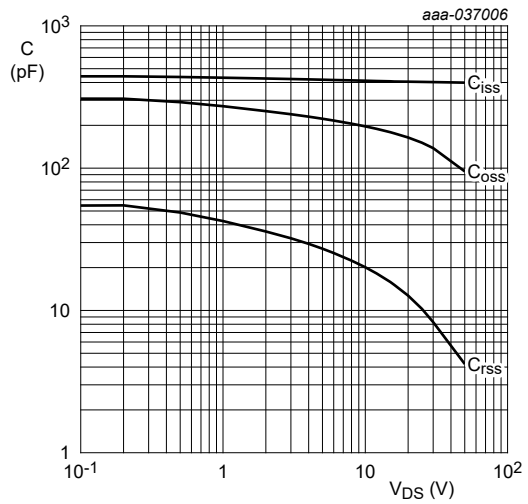



**Fig. 14. Gate charge waveform definitions**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

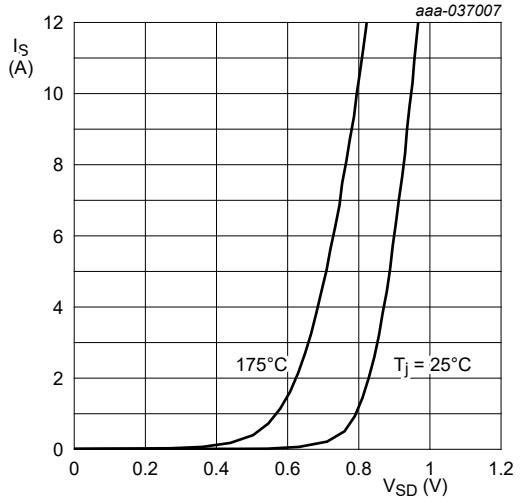



**Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

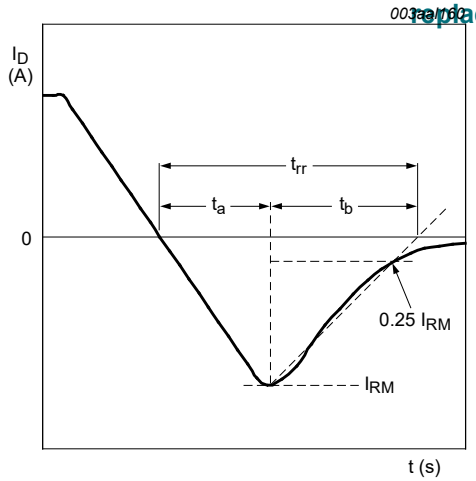
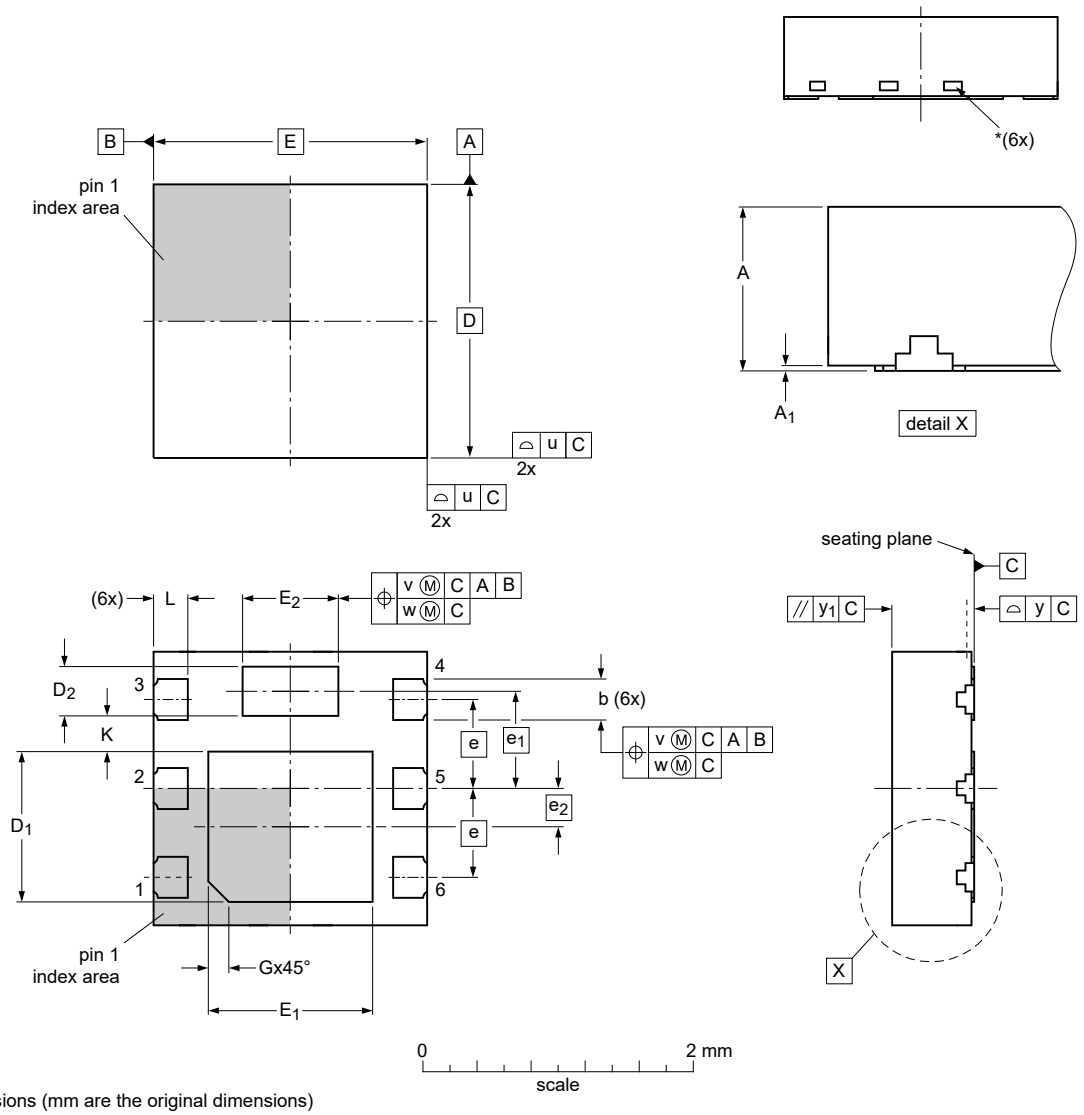



**Fig. 17. Reverse recovery timing definition**

# 11. Package outline

**DFN2020M-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm** **SOT1220-2**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | b | D | $D_1$ | $D_2$ | E | $E_1$ | $E_2$ | e | $e_1$ | $e_2$ | G | K | L | u | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | min | 0.55 | 0 | 0.25 | | 1.0 | 0.31 | | 1.1 | 0.6 | | | | | 0.2 | 0.20 | | | | | |
| | nom | 0.60 | 0.02 | 0.30 | 2 | 1.1 | 0.36 | 2 | 1.2 | 0.7 | 0.65 | 0.71 | 0.28 | 0.15 (ref) | | 0.25 | 0.05 | 0.1 | 0.05 | 0.05 | 0.05 |
| | max | 0.65 | 0.04 | 0.35 | | 1.2 | 0.41 | | 1.3 | 0.8 | | | | | | 0.30 | | | | | |

Note
1. Dimension A is including plating thickness.
2. * Visible depend upon used manufacturing technology.

*sot1220-2_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1220-2 | | --- | | | | ~~20-03-31~~ 20-04-01 |

**Fig. 18. Package outline DFN2020M-6 (SOT1220-2)**

## 12. Soldering

**Footprint information for reflow soldering of DFN2020M-6 package** **SOT1220-2**

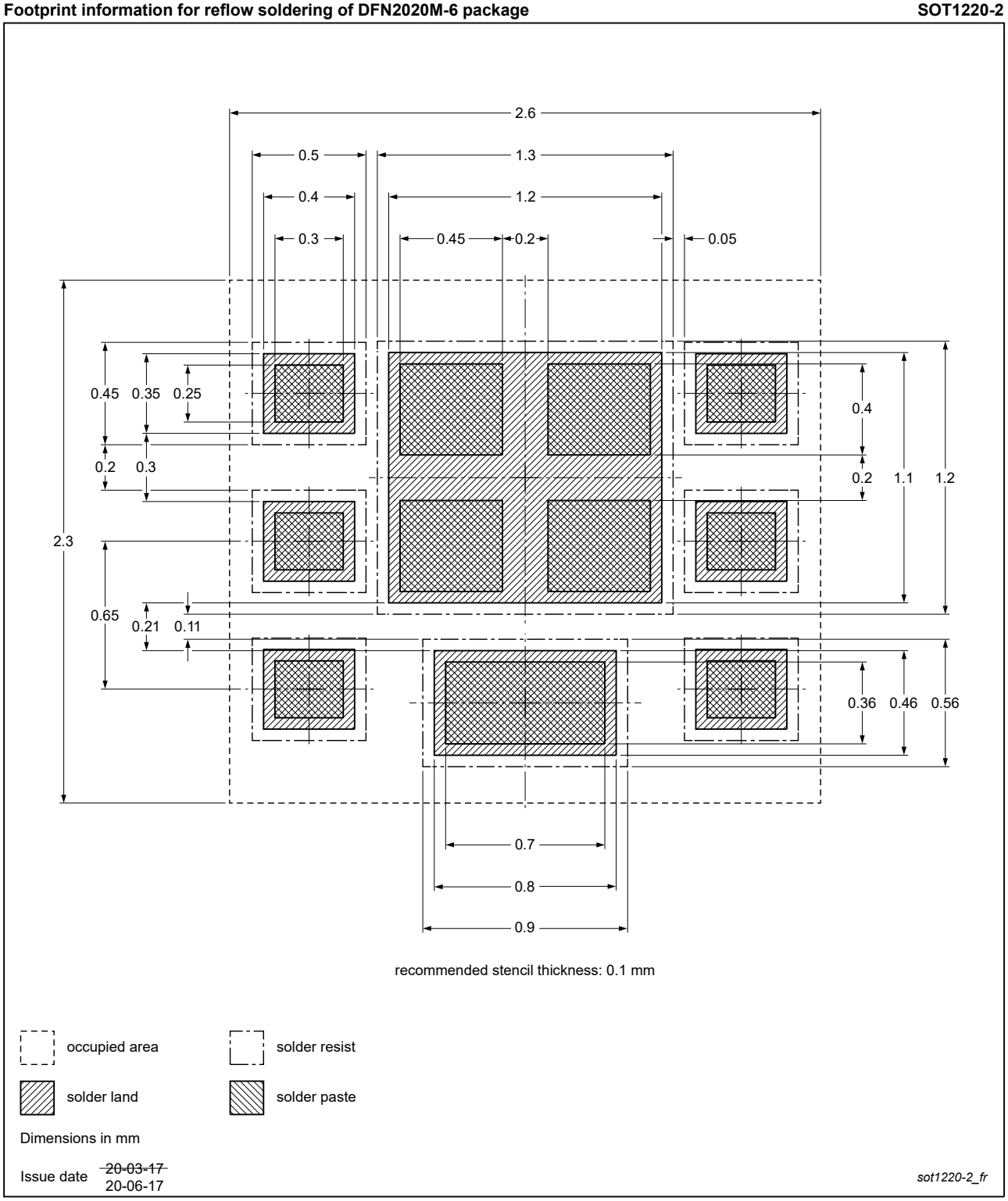



**Fig. 19. Reflow soldering footprint for DFN2020M-6 (SOT1220-2)**

# 13. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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N-channel 100 V, 82 mOhm standard level 'ASFET with enhanced SOA' in DFN2020 package. Recommended for fault tolerant applications including PoE, inrush management, eFuse and relay replacement

# Contents





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